# ADC : ADS1015

<http://www.ti.com/lit/ds/symlink/ads1015.pdf>

12-Bit ADC

The board has 2 ADC

|  |  |  |
| --- | --- | --- |
| **I2C Address** | **Communication** | **Analog Input** |
| **0B1001001** | ALERT/RDY, SDA, SCL | ADC1 = VCOUT BMS  ADC2 = VIOUT BMS  ADC3 = Thermistor R10  ADC4 = Thermistor R11 |
| **0B1001000** | ALERT/RDY, SDA, SCL | BQ24725A IOUT = 20x times the adapter(R19)/charger(R27)  Once VCC needs to be above UVLO and ACDET above 0.6V for IOUT to be valid |
| Comment | The inputs are the same physical signals on both ADC only the address differentiates them |  |

The ADS101x have two available conversion modes: single-shot and continuous-conversion.

## Typical Read/write

### Write a register

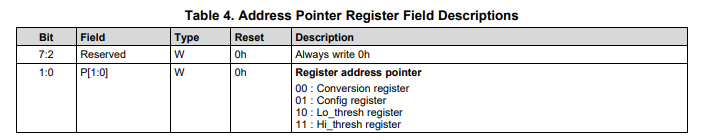
1. Write to Config register:
   * First byte: 0b10010000 (first 7-bit I 2C address followed by a low R/~~W~~ bit)
   * Second byte: 0b00000001 (points to Config register)
   * Third byte: 0b10000100 (MSB of the Config register to be written)
   * Fourth byte: 0b10000011 (LSB of the Config register to be written)

### Read a Register

1. Write to Address Pointer register:
   * First byte: 0b10010000 (first 7-bit I 2C address followed by a low R/~~W~~ bit)
   * Second byte: 0b00000000 (points to Conversion register)
2. Read Conversion register:
   * First byte: 0b10010001 (first 7-bit I 2C address followed by a high R/~~W~~ bit)
   * Second byte: the ADS101x response with the MSB of the Conversion register
   * Third byte: the ADS101x response with the LSB of the Conversion register

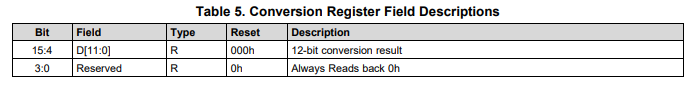
## Registers

Here is the different register

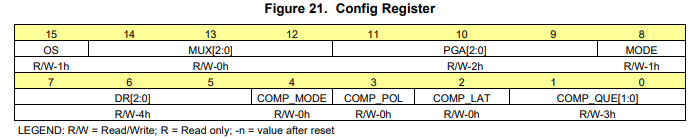


### Conversion Register

12bit conversion Result of asked input



### Config Register



Config we want

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 9** | **Bit 8** |
| 0 | 100 | | | 001 | | | 1 |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** |
| 100 | | | 0 | 0 | 0 | 1 | 1 |

Value in hex 0h4383

#### 15 OS

To start a conversion 0b1

#### 14:12 MUX (2:0) Control witch Input to measure

000 Diff between AIN0 and AIN1

001 Diff between AIN0 and AIN3

010 Diff between AIN1 and AIN3

011 Diff between AIN2 and AIN3

**100 Diff between AIN0 and GND SINGLE ENDED READ**

101 Diff between AIN1 and GND SINGLE ENDED READ

110 Diff between AIN2 and GND SINGLE ENDED READ

111 Diff between AIN3 and GND SINGLE ENDED READ

#### 11:9 PGA (2:0) Full scale range adjust

000 : FSR = ±6.144 V (1)

**001 : FSR = ±4.096 V (1)**

010 : FSR = ±2.048 V (default)

011 : FSR = ±1.024 V

100 : FSR = ±0.512 V

101 : FSR = ±0.256 V

110 : FSR = ±0.256 V

111 : FSR = ±0.256 V

#### 8 Mode

0 : Continuous-conversion mode

**1 : Single-shot mode or power-down state (default)**

#### 7:5 DR (2:0) Data rate for Continuous-conversion mode

000 : 128 SPS

001 : 250 SPS

010 : 490 SPS

011 : 920 SPS

**100 : 1600 SPS (default)**

101 : 2400 SPS

110 : 3300 SPS

111 : 3300 SPS

#### 4 COMP\_MODE Comparator mode

**0 : Traditional comparator (default)**

1 : Window comparator

#### 3 COMP\_POL Comparator polarity

**0 : Active low (default)**

1 : Active high

#### 2 CMOP\_LAT Latch comparator

**0 : Nonlatching comparator . The ALERT/RDY pin does not latch when asserted (default).**

1 : Latching comparator. The asserted ALERT/RDY pin remains latched until conversion data are read by the master or an appropriate SMBus alert response is sent by the master. The device responds with its address, and it is the lowest address currently asserting the ALERT/RDY bus line.

#### 1:0 CMOP\_QUE Number of event to trigger ALERT/RDY

00 : Assert after one conversion

01 : Assert after two conversions

10 : Assert after four conversions

**11 : Disable comparator and set ALERT/RDY pin to high-impedance (default)**

### Lo and High threshold register

Should not be used only used in single ended readings

# bq76925 Host-Controlled Analog Front End

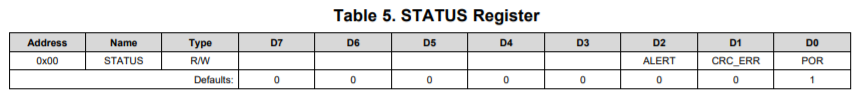
<http://www.ti.com/lit/ds/symlink/bq76925.pdf>

I2C address

0b01XXXXX where XXXXX is the register address

## Registers

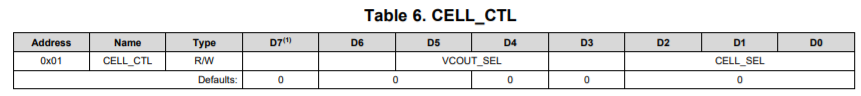
### 0b0100000 Status Register

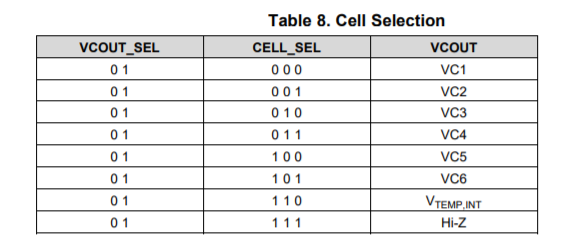
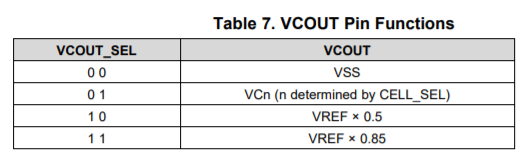


* ALERT: Over-current alert. Reflects state of the over-current comparator. ‘1’ = over-current.
* DCRC\_ERR: CRC error status. Updated on every I 2C write packet when CRC\_EN = ‘1’. ‘1’ = CRC error.
* POR: Power on reset flag. Set on each power-up and wake-up from sleep. May be cleared by writing with ‘0’

### 0b0100001 CELL\_CTL

Register where you can express which output you want on VCOUT



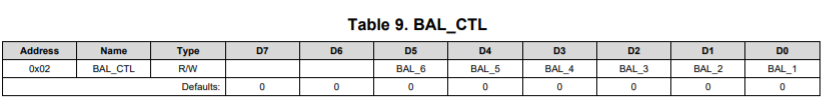


In to sweep all battery voltage the fallow instruction should be done

* 1. Write to access the front-end CELL\_CTL 0100001W
  2. Write to CELL\_CTL 00001000 (VOUT = VC1)
  3. Read ADC ADC1
  4. Repeat 1 to 3 but for other VCX

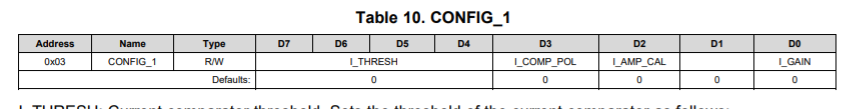
### 0b0100002 BAL\_CTL

This register is in charge to bypass batteries when charging

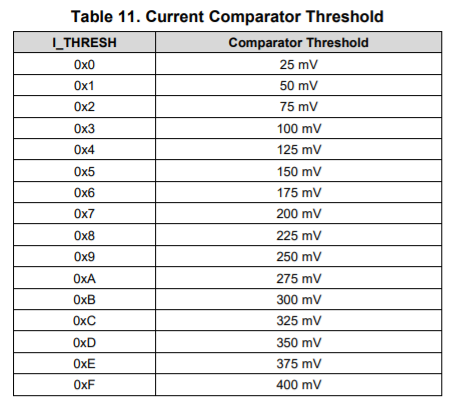


### 0b0100003 BAL\_CTL

This register is able to monitor the current while charging and discharging and send a flag if something is not normal



I\_THRESH: Current comparator between SENSN and SENSP threshold. Sets the threshold of the current comparator as follows:



I\_COMP\_POL: Current comparator polarity select. When ‘0’, trips on discharge current (SENSEP > SENSEN). When ‘1’, trips on charge current (SENSEP < SENSEN).

I\_AMP\_CAL: Current amplifier calibration. When ‘0’, current amplifier reports SENSEN with respect to VSS. When ‘1’, current amplifier reports SENSEP with respect to VSS. This bit can be used for offset cancellation as described under OPERATIONAL OVERVIEW.

I\_GAIN: Current amplifier gain. Sets the nominal gain of the current amplifier as follows

